REMARKS

The Examiner is thanked for the indication that claims 1-13, 22-32, and 34-37 are allowed and claims 19 and 20 are allowable if rewritten in independent form.

Claims 1-37 remain pending in the instant application. Claims 14-18, 21, and 33 presently stand rejected. Reconsideration of the pending claims are respectfully requested.

Claim Rejections – 35 U.S.C. § 102

Claims 14-18, 21, and 33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ooishi (US 6,404,258). Applicants respectfully traverse the rejections.

A claim is anticipated only if each and every element of the claim is found in a single reference. M.P.E.P § 2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the claim." M.P.E.P. § 2131 (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226 (Fed. Cir. 1989)).

Independent claim 14 recites, in pertinent parts,

> a clock enable circuit including:
> a clock input to receive a reference clock signal;
> an enable input;
> a circuit output to output a delayed clock signal being a delayed response to the reference clock signal;
> a **NAND logic circuit** having a **first NAND input coupled to receive the reference clock signal**, a **second NAND input coupled to the enable input**, and a NAND output; and
> an inverter circuit coupling the NAND output to the circuit output;
> ...

Applicants respectfully submit that Ooishi fails to disclose a NAND logic circuit having first and second inputs coupled as recited in claim 14.

Referring to FIG. 38 of Ooishi, the Examiner cites inverting circuit IVa as corresponding to the claimed NAND logic circuit, cites DIN as corresponding to the clock input for receiving a reference clock signal, and terminal 100d (VN) as corresponding to the enable input. Claim 14 recites that the NAND logic circuit includes first NAND input coupled to receive the reference clock signal and a second NAND input coupled to the enable input. Applicants respectfully submit that inverting circuit

IVa illustrated in FIG. 38 of Ooishi does not logically NAND DIN and terminal 100d (VN), as would be required per claim 14 according to the Examiner's interpretation.

To be sure, table 1 below illustrates a truth table for a NAND logic function.

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Table 1

However, the logic function implemented at circuit node 101, the output of inverting circuit IVa, based on inputs DIN and terminal 100d (VN), is not a NAND function, as can be seen by table 2.

(DIN)	(VN)	NODE 101
0	0	1
0	1	1
1	0	High Impedance State
1	1	0

Table 2

As can be seen from FIG. 38 and table 2 above, the [1,0] input combination for [DIN,VN] would result in a high impedance state at circuit node 101. This is because a '0' input to the gate of transistor 100d open circuits transistor 100d and would prevent inverting circuit IVa from being able to pull node 101 down to ground. Accordingly, inverting circuit IVa does not implement a logical NAND function of the variables DIN and VN (or the terminal 100d) and therefore cannot be interpreted to represent a "NAND logic circuit", as recited in claim 14. (Note, table 2 assumes transistor 100a is always close circuited, else the [0,0] and the [0,1] states would also be high impedance states in table 2.)

Consequently, Ooishi fails to disclose each and every element of claim 14, as required under M.P.E.P. § 2131. Accordingly, Applicants request that the instant §102 rejection of claim 14 be withdrawn.

The dependent claims are novel over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant § 102 rejections for the dependent claims be withdrawn.

CONCLUSION

In view of the foregoing remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

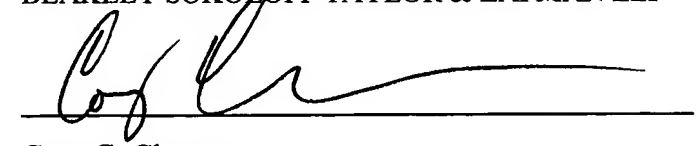
CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: Jan. 23, 2006



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